117/92, 93, 102, 103

10/615,632

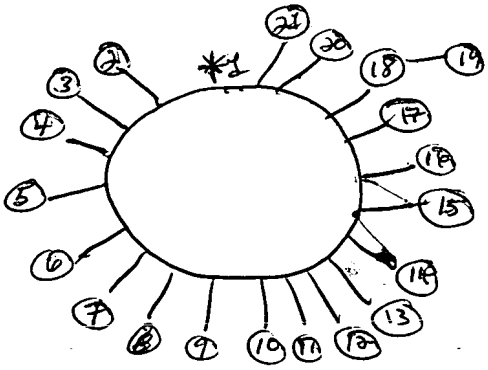
Examiner's Notes

*Priority document not recvd. TAIWAN 091124157 filed 10/26/2002;

S(MOCVD or metal(w)organic(w)chemical(w)vapor(w)deposition)
S(GaN or gallium(w)nitride
S(rapid(w)thermal(w)chemical(w)vapor(w)deposition)
VS (silicon(4a) substrate)

S(remov? or eliminat?)(GaN)(oxide(2w)layer)
VS(silicon(us)substrate)

S(SiCN or silicon(w)carbon(w)Nitride)
VS(grow? or deposit? or produc? or manufactur?)
S(pressure and temperature
S(H2 or hydrogen and SiH4 and NH3 or ammonia and C3H8)
S(rotat?)(GaN substrate#)



Motivation: In order to provide a method of growing silicon carbon nitride (SiCN) film as buffer layer to help grow GaN elements, & to break through bottleneck of hetero-structure epitaxy technology.

6,844,227

Search History

STN
(HCAPLUS, USPATALL, INSPEC, JAPIO)
3/8/05

=> d l12 1-2 abs,bib

L12 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2005 ACS on STN

AB A method of growing single crystal Ga nitride on **Si substrate** is given including: **removing oxide layer** of **Si substrate**, **growing buffer layer** of **Si** C nitride (**SiCN**), and **growing** single crystalline Ga nitride thin film, characterized in that a **buffer layer** of **SiCN** is **grown** to avoid lattice mismatch which appears when Ga nitride is grown directly on **Si substrate**, and that rapid thermal CVD is adopted to **grow SiCN buffer layer**, and that metalorg. CVD is adopted to **grow** single crystalline GaN thin film. The method has advantages: (a) eliminating lattice mismatch between GaN and Si effectively, (b) taking the place of sapphire substrate which has high lattice mismatch, and SiC substrate which is expensive, (c) integrating with maturely-developed, cheap Si semiconductor industry, (d) being compatible with VLSI technol., (e) being fabricated in large area substrate, (f) no need of isolated etching, (g) smaller dimension of each unit GaN element, (h) convenience to fabricate vertical-structured LED or LD element, (i) promoting GaN elements quality, (j) increasing yield and (k) reducing manufacturing cost,.

AN 2004:331399 HCAPLUS

DN 140:347950

TI Method of growing single crystal **gallium nitride** on **silicon substrate**

IN Fang, Yean Kuen; Chang, Wen Rong; Ting, Shyh Fann; Kuan, Hon; Chang, Cheng Nan

PA Taiwan

SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004074437	A1	20040422	US 2003-615632	20030708
	TW 574762	B	20040201	TW 2002-91124151	20021016
	JP 2004140354	A2	20040513	JP 2003-344337	20031002
PRAI	TW 2002-91124151	A	20021016		

L12 ANSWER 2 OF 2 USPATFULL on STN

AB A method of growing single crystal **Gallium Nitride** on **silicon substrate** is disclosed including: **removing oxide layer** of **silicon substrate**, **growing buffer layer** of **Silicon Carbon Nitride** (**SiCN**), and **growing** single crystalline Gallium Nitride thin film, characterized in that a **buffer layer** of **SiCN** is **grown** to avoid lattice mismatch which appears when **Gallium Nitride** is grown directly on **silicon substrate**, and that Rapid Thermal Chemical Vapor Deposition is adopted to **grow SiCN buffer layer**, and that Metalorganic Chemical Vapor Deposition is adopted to grow single crystalline GaN thin film. The method of present invention has advantages:

(a) eliminating lattice mismatch between GaN and Si effectively,

(b) taking the place of sapphire substrate which has high lattice mismatch, and SiC substrate which is expensive,

(c) integrating with maturely-developed, cheap silicon semiconductor

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=> d his

     (FILE 'HOME' ENTERED AT 12:44:31 ON 08 MAR 2005)

     FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 12:44:58 ON
     08 MAR 2005
L1        40808 S (MOCVD OR METALORGANIC(W)CHEMICAL(W)VAPOR(W)DEPOSITION)
L2        56938 S (GAN OR GALLIUM(W)NITRIDE)
L3         9676 S (GAN OR GALLIUM(W)NITRIDE)(6A)(SUBSTRATE)
L4       266837 S (SI OR SILICON)(4A)(SUBSTRATE)
L5        22017 S (REMOV? OR ELIMINAT?)(8A)(OXIDE(W)LAYER)
L6         1307 S (SICN OR SILICON(W)CARBON(W)NITRIDE)
L7        11252 S (GROW? OR PRODUC? OR MANUFACTUR? OR CREAT?)(8A)(BUFFER(W)LAYE
L8      1125477 S (PRESSURE AND TEMPERATURE)
L9       269782 S (H2 OR HYDROGEN AND SIH4 AND NH3 OR AMMONIA AND C3H8)
L10       32128 S (ROTAT?)(6A)(SUBSTRATE)
L11      291024 S  ABS
L12           2 S L3 AND L4 AND L5 AND L6 AND L7

=> s l6 and l7
L13           8 L6 AND L7

=> d l13 1-8 abs,bib

L13  ANSWER 1 OF 8  HCAPLUS  COPYRIGHT 2005 ACS on STN
AB   Low-temperature growth of SiCN nanoparticle films on an AlN
     buffer layer on Si(100) by consecutive RF magnetron
     sputtering is reported.  The visible photoluminescence (PL) is observed
     between 620 and 670 nm using a single photo excitation at 514.5 nm.  The
     growth of film at room temperature is found to yield the strongest PL
intensity,
     whereas the film grown at 200°C corresponds to the lowest PL
     intensity.  A similar variation of SiC diffraction intensity is also observed
     in XRD spectra.  The photoluminescence of the SiCN film is
     discussed on the base of the morphol., structural and elemental analyze.
AN   2005:173665  HCAPLUS
TI   LOW-TEMPERATURE GROWTH AND PHOTOLUMINESCENCE OF SiCN
     NANOPARTICLE FILM BY CONSECUTIVE RF MAGNETRON SPUTTERING
AU   Xu, M.; Ng, V. M.; Huang, S. Y.; Xu, S. Y.
CS   Plasma Sources and Applications Center, NIE, Nanyang Technological
     University, 1 Nanyang Walk, Singapore, 637616, Singapore
SO   Surface Review and Letters (2004), 11(6), 515-519
     CODEN: SRLEFH; ISSN: 0218-625X
PB   World Scientific Publishing Co. Pte. Ltd.
DT   Journal
LA   English

L13  ANSWER 2 OF 8  HCAPLUS  COPYRIGHT 2005 ACS on STN
AB   A method of growing single crystal Ga nitride on Si substrate is given
     including: removing oxide layer of Si substrate, growing
     buffer layer of Si C nitride (SiCN), and
     growing single crystalline Ga nitride thin film, characterized in that
     a buffer layer of SiCN is grown to
     avoid lattice mismatch which appears when Ga nitride is grown directly on
     Si substrate, and that rapid thermal CVD is adopted to grow
     SiCN buffer layer, and that metalorg. CVD is
     adopted to grow single crystalline GaN thin film.  The method has
     advantages: (a) eliminating lattice mismatch between GaN and Si
     effectively, (b) taking the place of sapphire substrate which has high
     lattice mismatch, and SiC substrate which is expensive, (c) integrating
     with maturely-developed, cheap Si semiconductor industry, (d) being
     compatible with VLSI technol., (e) being fabricated in large area
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industry,

(d) being compatible with VLSI technology,

(e) being fabricated in large area substrate,

(f) no need of isolated etching,

(g) smaller dimension of each unit GaN element,

(h) convenience to fabricate vertical-structured LED or LD element,

(i) promoting GaN elements quality,

(j) increasing yield

(k) reducing manufacturing cost,

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:98589 USPATFULL
TI Method of growing single crystal **Gallium Nitride** on **silicon substrate**
IN Fang, Yean Kuen, Tainan, TAIWAN, PROVINCE OF CHINA
Chang, Wen Rong, Yongkang City, TAIWAN, PROVINCE OF CHINA
Ting, Shyh Fann, Gangshan, TAIWAN, PROVINCE OF CHINA
Kuan, Hon, Tainan City, TAIWAN, PROVINCE OF CHINA
Chang, Cheng Nan, Sinshih Township, TAIWAN, PROVINCE OF CHINA
PI US 2004074437 A1 20040422
AI US 2003-615632 A1 20030708 (10)
PRAI TW 2002-91124151 20021016
DT Utility
FS APPLICATION
LREP PRO-TECHTOR INTERNATIONAL, 20775 Norada Court, Saratoga, CA, 95070-3018
CLMN Number of Claims: 21
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 305
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

=> d his

(FILE 'HOME' ENTERED AT 12:44:31 ON 08 MAR 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 12:44:58 ON 08 MAR 2005
L1 40808 S (MOCVD OR METALORGANIC(W)CHEMICAL(W)VAPOR(W)DEPOSITION)
L2 56938 S (GAN OR GALLIUM(W)NITRIDE)
L3 9676 S (GAN OR GALLIUM(W)NITRIDE)(6A)(SUBSTRATE)
L4 266837 S (SI OR SILICON)(4A)(SUBSTRATE)
L5 22017 S (REMOV? OR ELIMINAT?)(8A)(OXIDE(W)LAYER)
L6 1307 S (SICN OR SILICON(W)CARBON(W)NITRIDE)
L7 11252 S (GROW? OR PRODUC? OR MANUFACTUR? OR CREAT?)(8A)(BUFFER(W)LAYE
L8 1125477 S (PRESSURE AND TEMPERATURE)
L9 269782 S (H2 OR HYDROGEN AND SIH4 AND NH3 OR AMMONIA AND C3H8)
L10 32128 S (ROTAT?)(6A)(SUBSTRATE)
L11 291024 S ABS
L12 2 S L3 AND L4 AND L5 AND L6 AND L7

=>

substrate, (f) no need of isolated etching, (g) smaller dimension of each unit GaN element, (h) convenience to fabricate vertical-structured LED or LD element, (i) promoting GaN elements quality, (j) increasing yield and (k) reducing manufacturing cost,.

AN 2004:331399 HCAPLUS
DN 140:347950
TI Method of growing single crystal gallium nitride on silicon substrate
IN Fang, Yean Kuen; Chang, Wen Rong; Ting, Shyh Fann; Kuan, Hon; Chang, Cheng Nan
PA Taiwan
SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004074437	A1	20040422	US 2003-615632	20030708
	TW 574762	B	20040201	TW 2002-91124151	20021016
	JP 2004140354	A2	20040513	JP 2003-344337	20031002
PRAI	TW 2002-91124151	A	20021016		

L13 ANSWER 3 OF 8 INSPEC (C) 2005 IEE on STN
AN 2001:7045950 INSPEC DN A2001-21-8115H-007
AB A nonvapor-liquid-solid (VLS) method of growing high-purity **silicon carbon nitride** (SiCxNy) nanorods with rod widths ranging from 10 to 60 nm and lengths of microns is reported. Unlike the case for ordinary VLS or catalyst-mediated growth, the two-stage process is a catalyst-free approach since it does not involve any catalyst during growth of the nanorods. The first stage involves formation of a buffer layer containing various densities of SiCxNy nanocrystals by electron cyclotron resonance plasma enhanced chemical vapor deposition (PECVD); whereas the second stage involves a high growth rate along a preferred orientation to produce high-aspect-ratio nanorods using microwave PECVD. Moreover, the number density and diameter of the nanorods can be controlled by the number density and size of the nanocrystals in the **buffer layer**. **Production** of quasi-aligned SiCxNy nanorods with a number density of the rods as high as 1010 cm-2 has been achieved. The SiCxNy nanorods thus produced exhibit good field emission characteristics with stable operation over 8 h. The approach provides a new advance to synthesize nanorod materials in a controllable manner.
DN A2001-21-8115H-007
TI Catalyst-free and controllable growth of SiCxNy nanorods.
AU Chen, L.C. (Center for Condensed Mater. Sci., Nat. Taiwan Univ., Taipei, Taiwan); Chang, S.W.; Chang, C.S.; Wen, C.Y.; Wu, J.-J.; Chen, Y.F.; Huang, Y.S.; Chen, K.H.
SO Journal of the Physics and Chemistry of Solids (Sept.-Oct. 2001) vol.62, no.9-10, p.1567-76. 42 refs.
Doc. No.: S0022-3697(01)00096-8
Published by: Elsevier
Price: CCCC 0022-3697/2001/$20.00
CODEN: JPCSAW ISSN: 0022-3697
SICI: 0022-3697(200109/10)62:9/10L.1567:CFCG;1-9
DT Journal
TC Experimental
CY United Kingdom
LA English

L13 ANSWER 4 OF 8 USPATFULL on STN
AB In a field effect transistor, an Si layer 11, an SiC (Si.sub.1-yC.sub.y) channel layer 12, a CN gate insulating film 13 made of a carbon nitride layer (CN) and a gate electrode 14 are deposited in this order on an Si

substrate 10. The thickness of the SiC channel layer 12 is set to a value that is less than or equal to the critical thickness so that a dislocation due to a strain does not occur according to the carbon content. A source region 15 and a drain region 16 are formed on opposite sides of the SiC channel layer 12, and a source electrode 17 and a drain electrode 18 are provided on the source region 15 and the drain region 16, respectively.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:290099 USPATFULL
TI Semiconductor devices and method for manufacturing the same
IN Kubo, Minoru, Mie, JAPAN
Ichikawa, Yo, Aichi, JAPAN
Asai, Akira, Osaka, JAPAN
Kawashima, Takahiro, Osaka, JAPAN
PA Matsushita Electric Industrial Co., Ltd., Osaka, JAPAN (non-U.S. corporation)
PI US 2004227169 A1 20041118
AI US 2004-868774 A1 20040617 (10)
RLI Division of Ser. No. US 2002-203891, filed on 15 Aug 2002, PENDING A 371 of International Ser. No. WO 2001-JP11504, filed on 26 Dec 2001, UNKNOWN
PRAI JP 2000-395824 20001226
DT Utility
FS APPLICATION
LREP NIXON PEABODY, LLP, 401 9TH STREET, NW, SUITE 900, WASHINGTON, DC, 20004-2128
CLMN Number of Claims: 29
ECL Exemplary Claim: 1
DRWN 24 Drawing Page(s)
LN.CNT 2620
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 5 OF 8 USPATFULL on STN
AB A method of growing single crystal Gallium Nitride on silicon substrate is disclosed including: removing oxide layer of silicon substrate, **growing buffer layer** of **Silicon Carbon Nitride** (**SiCN**), and **growing** single crystalline Gallium Nitride thin film, characterized in that a **buffer layer** of **SiCN** is **grown** to avoid lattice mismatch which appears when Gallium Nitride is grown directly on silicon substrate, and that Rapid Thermal Chemical Vapor Deposition is adopted to **grow SiCN buffer layer**, and that Metalorganic Chemical Vapor Deposition is adopted to grow single crystalline GaN thin film. The method of present invention has advantages:

(a) eliminating lattice mismatch between GaN and Si effectively,

(b) taking the place of sapphire substrate which has high lattice mismatch, and SiC substrate which is expensive,

(c) integrating with maturely-developed, cheap silicon semiconductor industry,

(d) being compatible with VLSI technology,

(e) being fabricated in large area substrate,

(f) no need of isolated etching,

(g) smaller dimension of each unit GaN element,

(h) convenience to fabricate vertical-structured LED or LD element,

(i) promoting GaN elements quality,

(j) increasing yield

(k) reducing manufacturing cost,

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:98589 USPATFULL
TI Method of growing single crystal Gallium Nitride on silicon substrate
IN Fang, Yean Kuen, Tainan, TAIWAN, PROVINCE OF CHINA
Chang, Wen Rong, Yongkang City, TAIWAN, PROVINCE OF CHINA
Ting, Shyh Fann, Gangshan, TAIWAN, PROVINCE OF CHINA
Kuan, Hon, Tainan City, TAIWAN, PROVINCE OF CHINA
Chang, Cheng Nan, Sinshih Township, TAIWAN, PROVINCE OF CHINA
PI US 2004074437 A1 20040422
AI US 2003-615632 A1 20030708 (10)
PRAI TW 2002-91124151 20021016
DT Utility
FS APPLICATION
LREP PRO-TECHTOR INTERNATIONAL, 20775 Norada Court, Saratoga, CA, 95070-3018
CLMN Number of Claims: 21
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 305
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 6 OF 8 USPATFULL on STN
AB In a field effect transistor, an Si layer 11, an SiC (Si.sub.1-yC.sub.y) channel layer 12, a CN gate insulating film 13 made of a carbon nitride layer (CN) and a gate electrode 14 are deposited in this order on an Si substrate 10. The thickness of the SiC channel layer 12 is set to a value that is less than or equal to the critical thickness so that a dislocation due to a strain does not occur according to the carbon content. A source region 15 and a drain region 16 are formed on opposite sides of the SiC channel layer 12, and a source electrode 17 and a drain electrode 18 are provided on the source region 15 and the drain region 16, respectively.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:150830 USPATFULL
TI Semiconductor device and its manufacturing method
IN Kubo, Minoru, Mie, JAPAN
Ichikawa, Yo, Aichi, JAPAN
Asai, Akira, Osaka, JAPAN
Kawashima, Takahiro, Osaka, JAPAN
PI US 2003102490 A1 20030605
US 6844227 B2 20050118
AI US 2002-203891 A1 20020815 (10)
WO 2001-JP11504 20011226
PRAI JP 2000-395824 20001226
DT Utility
FS APPLICATION
LREP Nixon Peabody, 8180 Greensboro Drive Suite 800, McLean, VA, 22102
CLMN Number of Claims: 31
ECL Exemplary Claim: 1
DRWN 24 Drawing Page(s)
LN.CNT 2627
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 7 OF 8 USPATFULL on STN
AB A photovoltaic device having a pin type semiconductor junction in which a p-type semiconductor layer and an n-type semiconductor layer are

laminated with an interposed i-type semiconductor layer, comprises at least one doped layer of a non-monocrystal semiconductor disposed under and/or over the i-type semiconductor layer, wherein the at least one doped layer has a surface exposed to a plasma containing a band gap increasing element.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 1998:14343 USPATFULL
TI Photovoltaic device and method of manufacturing the same
IN Matsuyama, Jinsho, Kyoto, Japan
Hayashi, Ryo, Tsukuba, Japan
PA Canon Kabushiki Kaisha, Tokyo, Japan (non-U.S. corporation)
PI US 5716480 19980210
AI US 1996-678701 19960711 (8)
PRAI JP 1995-177437 19950713
JP 1995-177438 19950713
JP 1995-177439 19950713
JP 1995-177440 19950713
JP 1995-177441 19950713
DT Utility
FS Granted
EXNAM Primary Examiner: Weisstuch, Aaron
LREP Fitzapatrick, Cella, Harper & Scinto
CLMN Number of Claims: 122
ECL Exemplary Claim: 1,8
DRWN 7 Drawing Figure(s); 7 Drawing Page(s)
LN.CNT 3671
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 8 OF 8 USPAT2 on STN
AB In a field effect transistor, an Si layer, an SiC (Si.sub.1-yC.sub.y) channel layer, a CN gate insulating film made of a carbon nitride layer (CN) and a gate electrode are deposited in this order on an Si substrate. The thickness of the SiC channel layer is set to a value that is less than or equal to the critical thickness so that a dislocation due to a strain does not occur according to the carbon content. A source region and a drain region are formed on opposite sides of the SiC channel layer, and a source electrode and a drain electrode are provided on the source region and the drain region, respectively.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:150830 USPAT2
TI Semiconductor devices and method for manufacturing the same
IN Kubo, Minoru, Mie, JAPAN
Ichikawa, Yo, Aichi, JAPAN
Asai, Akira, Osaka, JAPAN
Kawashima, Takahiro, Osaka, JAPAN
PA Matsushita Electric Industrial Co., Ltd., Osaka, JAPAN (non-U.S. corporation)
PI US 6844227 B2 20050118
WO 2002005265 20020704
AI US 2002-203891 20020815 (10)
WO 2001-JP11504 20011226
20020815 PCT 371 date
PRAI JP 2000-395824 20001226
DT Utility
FS GRANTED
EXNAM Primary Examiner: Jackson, Jerome
LREP Nixon Peabody, LLP, Studebaker, Donald
CLMN Number of Claims: 1
ECL Exemplary Claim: 1
DRWN 48 Drawing Figure(s); 24 Drawing Page(s)
LN.CNT 2425

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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